REMARKS

Claims 2 through 8, 10 and 12 through 21 are now pending. In response to the non-final Office Action dated June 23, 2006, claims 1, 9 and 11 are cancelled and claims 2 through 5, 10 12, 13 and 18 are amended. Care has been taken to avoid entry of new matter. A petition for one month extension of the period for response, with appropriate fee charge authorization, is filed herewith. Favorable reconsideration of the application is respectfully solicited.

Claims 1, 9, 11, 18 and 20 were rejected under the first paragraph of 35 U.S.C. § 112 for lacking enabling disclosure of control for switching the current driving capability of the driving unit according to a variation in the amount of current required by the load. This holding is based on a lack of feedback shown in Fig. 3. The Office Action concludes that undue experimentation would be necessitated by the artisan trying to make and use the invention.

The rejection is respectfully traversed. It is submitted that the specification sufficiently describes how to design the control unit and that the invention is described sufficiently to enable one skilled in the pertinent art to make and use the invention. For example, the specification describes:

(At lines 9-24 of page 13) The control unit 88 switches the current driving capability of the entire driving unit 80 by controlling the number of circuits to operate out of the first bias circuit 82 and the second bias circuit 84. For example, in a period when the first conversion unit 22 requires a relatively high current, both the first bias circuit 82 and the second bias circuit 84 are operated. In a period when a relatively low current is sufficient, either one of the first bias circuit 82 and the second bias circuit 84 is operated. The current driving capabilities of the first bias circuit 82 and the second bias circuit 84, and the control timing of the control unit 88 on the third transistor Tr3, the sixth transistor Tr6, the first output transistor Tr10, and the second output

transistor Tr20 are designed in accordance with the variation in the amount of current required in the first conversion unit 22 to which the bias voltage is applied (emphasis supplied).

(At line 25 of page 13 - line 22 of page 14) Fig. 4 is a time chart showing the relationship between a change of operation of the first conversion unit 22 and the control of the control unit 88 according to the first embodiment. Starting from the top, the chart shows the operation mode of the first amplifier circuit 38 included in the first conversion unit 22, the on/off timing of the third transistor Tr3, and the on/off timing of the sixth transistor Tr6. Hereinafter, the on/off timing of the third transistor Tr3 shall also represent the on/off timing of the first output transistor Tr10, and the on/off timing of the sixth transistor Tr6 the on/off timing of the second output transistor Tr20. The first amplifier circuit 38 repeats an auto-zero operation and an amplification operation alternately. In the present embodiment, a relatively high current is required in the period of the auto-zero operation, and a relatively low current is sufficient in the period of the amplification operation. On this account, the control unit 88 turns on both the third transistor Tr3 and the sixth transistor Tr6 in the period of the auto-zero operation. In the period of the amplification operation, the control unit 88 turns off the third transistor Tr3 and keeps the sixth transistor Tr6 alone turned on. This allows a fine adjustment to the power consumption of the circuit which applies the bias voltage (emphasis supplied).

These paragraphs clearly describe how the control unit switches the current driving capability of the driving unit according to a variation in the amount of current required by the load. Further, Fig. 8 exemplifies a circuit of the control unit 88. Therefore, the disclosure does not require an artisan to perform undue experimentation to make and use the invention. Withdrawal of the rejection is respectfully solicited.

Claims 18 and 20 have not been rejected on the basis of prior art. Claims 19 and 21, which are dependent, respectively, from claims 18 and 20, were indicated to contain allowable subject matter. It is submitted, therefore, that claims 18 through 21 are now allowable.

Claim 5 was rejected under the second paragraph of 35 U.S.C. § 112. In response, claim 5 has been amended to change the phrase "CMOS transistor" to "CMOS transistor pair," as suggested in the Office Action. Withdrawal of the rejection is respectfully solicited.

Claims 1 and 3 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. patent 6,456,555 (Sim). In response, claim 1 has been cancelled and the rejection of claim 3, which has been rewritten in independent form, is respectfully traversed. It is submitted, for reasons discussed below, that Sim does not meet the requirements of claim 3.

Claim 3 recites, *inter alia*, the following:

> a plurality of bias circuits which are connected in parallel and have *the same current driving capability*, and
>
> the control unit switches the current driving capability by *controlling the number of circuits* to operate out of the plurality of bias circuits (emphasis supplied).

The Office Action states that resistance values 112, 113, 122 and 123 of Sim can be controlled to achieve the same current driving capability (lines 12-13 of page 4). However, contrary to this holding, Sim states "by controlling the resistance values 112 and 113 independently of resistors 122 and 123, reference voltages can be provided to obtain suitable target VPP levels for both the normal operation and high voltage test modes." That is, Sim does not provide any suggestion that the resistance values 112 and 113 and the resistance values 122 and 123 are associated and cooperatively controlled.

Rather, in Sim, the first reference voltage generating circuit 110 that includes the resistors 112 and 113 and the second reference voltage generating circuit 120 that includes the resistors

122 and 123 are selectively used in each corresponding mode. The first circuit 110 is driven in the test mode while the second circuit 120 is driven in the normal operation mode (line 25 of column 4 - line 5 of column 5). Sim thus requires that the first circuit 110 has a different characteristic from the second circuit 120 so as to be suitable for each corresponding mode. Thus, Sim does not disclose or suggest that "a plurality of bias circuits are connected in parallel and have the same current driving capability."

Further, the first circuit 110 and the second circuit 120 are not simultaneously controlled since each circuit is selectively controlled in each corresponding mode. Thus, Sim does not disclose or suggest "the control unit switches the current driving capability by controlling the number of circuits to operate out of the plurality of bias circuits."

Withdrawal of the rejection of claim 3, therefore, is respectfully solicited.

Claims 1, 4 and 11 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. published application 2004/0046684 (Cusinato). In response claims 1 and 11 have been cancelled and the rejection of claim 4, which has been amended to be dependent from now amended claim 2, is respectfully traversed. As parent claim 2 has not been rejected on the basis of Cusinato, the rejection of claim 4 is to be considered with the rejection of claim 2 as discussed below.

Claims 1, 2 and 9 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. patent 6,784,721 (Torrisi). In response, claims 1 and 9 have been cancelled and claim 2 has been amended to independent form with additional recitation. The rejection as it may be considered with respect to amended claim 2 is respectfully traversed.

Claim 2, in addition to containing the recitation of now cancelled parent claim 1 has been amended to further recite that the plurality of bias circuits output the same bias voltage. Torrisi

does not meet these claim requirements. In Torrisi, the first and second generators GL and GH in Fig. 6 are specifically illustrated in Fig. 10. The first generator GL comprises a first transistor Q1 and a first resistor R1 and the second generator GH comprises a second transistor Q2 and a second resistor R2 Thus, the first and second generators GL and GH respectively output different voltages. Thus claim 2 and its dependent claim 4 are patentably distinguishable. Claims 5 through 7, which also depend from claim 2, have been indicated to contain patentable subject matter. Withdrawal of the rejection is respectfully solicited.

In summary, the remaining rejected claims 2, 3, 5, 18 and 19 have been shown above to be patentably distinguishable. Withdrawal of the rejections and allowance of the application are respectfully solicited. To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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